**IN THE CLAIMS**

Please amend the claims as follows:

1. (Canceled)

2. (Currently amended) A memory trouble relief circuit for relieving a [[the]] failure of a memory of a semiconductor integrated circuit having the memory, the memory trouble relief circuit comprising:

a self-diagnosis circuit, which diagnoses the memory and outputs a [[the]] diagnosed result to an external power control circuit; and

a redundancy relief circuit, which have a redundancy circuit by which a [[the]] defective part of the memory is replaced based on the diagnosed result,

wherein a [[the]] supply of power to the redundancy relief circuit is controlled independently of a [[the]] supply of power to the semiconductor integrated circuit by the external power control circuit operating based on the diagnosed result.

3. (Canceled)

4. (Currently amended) A memory trouble relief circuit according to claim 2 [[1]], wherein the supply of power to the redundancy relief circuit is supplied from a power source different from that of the semiconductor integrated circuit.

5. (Currently amended) A memory trouble relief circuit according to claim 2, wherein the self-diagnosis circuit outputs the diagnosed result of the memory obtained every time a [[the]] power is turned on to the power control circuit.

6. (Canceled)

7. (Original) A memory trouble relief circuit according to claim 2, wherein the power control circuit is provided outside the semiconductor integrated circuit.

8. (Canceled)

9. (Currently amended) A power control method for a memory trouble relief circuit according to claim 2 [[1]], wherein power is supplied to the redundancy relief circuit only when the defective part of the memory is replaced by the redundancy circuit based on the diagnosed result of the memory.

10. (Currently amended) A power wiring method for a memory trouble relief circuit according to claim 2 [[1]], wherein a [[the]] power supply line for the redundancy relief circuit is cut by trimming when the defective part of the memory is not replaced by the redundancy circuit based on the diagnosed result of the memory.